REMARKS

Claims 1, 18, 21 and 22 are amended herein. Claims 1-14 and 18, 19, 21 and 22 remain pending in the application.

Finality of the Office Action

The Office Action is indicated as being Final. The Finality of the Office Action is improper since raising **numerous** new grounds within the rejections and arguments sections that the Applicant has not had an opportunity to respond to under a non-Final Office Action. The Applicant respectfully requests that the Finality of the Office Action be withdrawn.

In the Drawings

Fig. 2 was objected to as allegedly mislabeling drain-source voltage of switch MC in Fig. 1.

Applicant proposes to change Fig. 2 to match the description in the Specification. No new matter is added. It is respectfully requested that the proposed changes be approved and that the objection to the Drawings be withdrawn.

Objection to the Disclosure

The disclosure was again objected to for an alleged informality. In particular, the Examiner alleges that switch MC, described at page 7, line 18 of the disclosure should be labeled switch MS. The Examiner questions why MC is identified as a switch on lines 18 and 19, but as a current source on line 21.

From the Examiner's comments about the invention, the Examiner seems to be **misinterpreting** the operation of the invention. The Applicant is describing using the mirror path to equalize the current level on both sides of the **current source switch MC**. The switch MC is a switched current source. The Examiner's suggestion of changing the labeling of switch MC on page 7, lines 18 and 19 to switch MS would leave the paragraph erroneously descriptive of the invention.

Current flows into the circuit from the top of the Fig. 5 into the current switch MC. The current enters switch MC through switch MC's current source leg of the transistor. This is the current source side of the transistor.

All of the rest of the components in Fig. 5 are connected to the drain leg of the transistor MC. Since all of the other components act as a **load**, the **drain side** of current switching transistor MC is the load side.

The Examiner **AGAIN** questions how the Applicant equalizes something that is already equal, or substantially equal? In particular, the Examiner alleges that since current flowing through switch (transistor) MC will have minimal loss due to leakage current within the transistor, the current level at the source of MC is considered equal to the current level at its drain (Office Action, page 4).

As Applicant has **REPEATEDLY** tried to convey to the Examiner, charge injection is a current spike associated with switching of a **switched current source**. When a current source enters its saturation from a triod state, minority carriers from an inversion layer of the current source may be injected into a load capacitor (Specification, page 2, lines 1-11).

The Examiner questions (Office Action, page 16) what causes the current source switch to switch. The reason for switching is not part of the invention and is not at issue for the Examiner's review. The reason for switching is not claimed and is therefore moot.

The Examiner alleges that only when switch MC is combined with switches MS and/or MT would it be considered a switched current source by the Examiner (Office Action, page 16). The Applicant respectfully disagrees.

Switch MC is within the current path and controls current flow to the rest of the circuit including the load. Switch MC, acting **alone**, causes current to flow past its point within the circuit. All the switches are **not** required to act in concert to perform the function of a switched current source, as alleged by the Examiner. A current spike, i.e., charge injection, is release when a **switched current source** is switched, not requiring other switch components within the circuit to switch.

Withdrawal of the objection is **AGAIN** respectfully requested.

Section 112 rejection of Claims 1-14, 18, 19, 21 and 22

Claims 1-14, 18, 19, 21 and 22 were rejected under 35 USC 112, second paragraph. The Applicant respectfully traverses the rejection.

Claims 1, 18, 21 and 22

Claims 1, 18, 21 and 22 allegedly claim unclear language, i.e., "to equalize a current level produced by said current source". The Applicant is describing using a mirror path to **equalize** current levels on both sides of a current source, e.g., page 7, lines 17-22 of the Specification.

As discussed above, the Examiner seems to be **misinterpreting** the operation of the invention. The Examiner questions what the current source is equalized with respect to (Office Action, page 17). The current source is equalized with respect to **ITSELF**. A current source that is equalized has its own variations eliminated.

The Examiner repeatedly states there is no unequal state to be equalized, contrary to the Applicant's disclosure. The Examiner **AGAIN** questions that if the current source is providing a constant current, wouldn't that be considered equal to its desired operational current. Equalization does not simply mean operating a current source at its desired operational current, although that could possibly be the ultimate result of equalization. As discussed above, equalizing a current level produced by a current source **eliminates variations** within the current source, as described in the Specification at, e.g., page 7, lines 17-22.

Nowhere does Applicant claim an equalized current source or claim a circuit with currents on both sides of a current source being equal, contrary to the Examiner's assertion (Office Action, page 4). On the contrary, to equalize a current source, one must start with a current source that needs equalized, i.e., currents on both sides of a current source that are **NOT** equal. It would be nonsense to equalize something that the Examiner alleges is already equal. Charge injection is a current spike that is **UNEQUAL** and must be equalized.

The Examiner alleges that the Applicant's own Figs. do not show how current would flow in the pull-down path, and therefore is unclear how the current of the Applicant's own current source is equalized (Office Action, page 5).

The Examiner is requested review Fig. 5 and its accompanying text. The load can receive current through switch MS. Once switch MT is off and switch MS is on, all current will flow through the path through switch MS. Vise versa, once switch MS is off and switch MT is on, all current will flow through the pull down mirror path through switch MT. This allows load CL to **substantially** constantly receive current from the current source switch MC through switch MS. The load will not receive current during a **very** short period of time during charge injection when current is flowing in the mirror path.

Claims 21 and 22

The Office Action **AGAIN** alleges that the language "continuously receives said current flowing from said current source" is still misleading from claims 21 and 22. The Applicant respectfully disagrees.

A reading of the entire claim language indicates the limitation reads "**substantially** continuously receives said current flowing from said current source". The mirror path diverts the charge injection to ground when the switch at the current source is initially opened. Therefore, the load substantially continuously receives current since the charge injection only exists for a **very short time** when current switch initially allows current to flow to a load. The Examiner is ignoring the claim limitation as a **whole**. The Applicant is **NOT** claiming a load that "continuously" receives current, as the Examiner alleges, but is claiming a load that "**substantially continuously**" receives current.

The Applicants are claiming the invention broadly, as a current source. As the claims stand, the claims are clearly written as broadly claiming a current source. The invention is clearly disclosed in that the current source, e.g., current source MC and current source 420, are the current sources of the circuit.

The Examiner is requested to consider the claim language as a whole, and not as parts taken out of context. The Examiner is not giving weight to the claimed term "substantially".

The Examiner alleges that "the load will always receive the current flow from the current source unless the current is allowed to become fully charged, and at that time, current flow would then cease. Also, as long as switch 430 is closed, there will be no charge injection related to switch 430 because of the lack of switching operations" (Office Action, page 5).

Load 440 is depicted as a capacitor CL in Fig. 5. However, Fig. 4 shows any load as component 440 within the circuit. Capacitor CL show in Fig. 5 is for example purposes only, with one of ordinary skill in the art recognizing the Applicant's invention would be just as applicable with any load as component 440.

Moreover, as the Applicant has **repeatedly** tired to convey to the Examiner, the charge injection is associated with a switched current source, i.e., switched current source 420, **NOT** switch 430 as alleged by the Examiner.

Any claims not specifically addressed under 35 USC 112, second paragraph above are rejected based on dependency.

All the claims are in full conformance with 35 USC 112, and the Applicant requests the rejections be withdrawn.

Claims 1-5, 8-10, 12-19, 21 and 22 over Ravon

In the Office Action, claims 1-5, 8-10, 12, 18, 19, 21 and 22 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by US Patent No. 6,137,275 to Ravon ("Ravon"), and claims 13 and 14 are rejected as obvious over Ravon. The Applicant respectfully traverses the rejection as follows.

Claims 1-5, 8-10, 12-14, 18, 19, 21 and 22 recite, *inter alia,* a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered.

Ravon appears to teach a system for providing a regulated voltage meant to supply a load (Ravon, Abstract). A current source providing the maximum current likely to be surged by the load, and a device for receiving the constant current and regulating the load supply voltage (Ravon, Abstract). A source 11 provides a constant voltage to a load, within a maximum current value that the load is likely to consume (Ravon, col. 3, lines 35-43). A regulating

device 10 eliminates transients of the voltage supply to a load (Ravon, col. 3, lines 24-34). The regulating device includes a MOS power transistor M1, a MOS transistor M2, a transistor bias control circuit 13, and a comparator 14 (Ravon, Fig. 2; col. 3, line 49-col. 5, line 18). Transistor M2 controls the flow of current from the current source to ground (Ravon, Fig. 2). Transistor M1 controls the flow of current from the current source to the load (Ravon, Fig. 2).

Ravon's system is designed to supply a regulated voltage, at varying currents but within a maximum surge current (Ravon, col. 3, lines 35-44). The duel paths within Ravon's item 10 operate to limit transient variations of voltage Vout supplying a load, e.g., a microprocessor (Ravon, col. 3, lines 24-27). Ravon supplies an **uninterrupted** voltage and current supply. Ravon's elimination of voltage variations in an **uninterrupted** voltage and current supply is **NOT** a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered, as claimed by claims 1-5, 8-10, 12-14, 18, 19, 21 and 22.

Charge injection relates to the current spike that occurs most frequently during a switch state of either a MOS transistor switch or, more seriously, when a current source enters its saturation from a triod state, minority carriers from the inversion layer of the current source may be injected into the load. Ravon teaches the purpose of MOS transistor M2 is to absorb excess current during periods when the load only requires a low supply current. Ravon's **uninterrupted** current source is not taught as even being capacitive, and producing current spikes during **switching**. Ravon's **load** is creating the current fluctuations. **Loads do not create charge injection**. Reducing excess current during periods when the load only requires a low supply current (col. 3, lines 59-62) is **NOT** charge injection during **switching** of a current source while the current source remains powered, as claimed by claims 1-5, 8-10, 12-14, 18, 19, 21 and 22.

The Examiner rejected claims 1-5, 8-10, 12-14, 18, 19, 21 and 22 as being anticipated by Ravon. Therefore, Ravon **MUST** teach reducing charge injection by a pull-down mirror path, as claimed by claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22. Charge injection, as claimed by claims 1-5, 8-10, 12-14, 18,

19, 21 and 22, is a **term of art** associated with a **switched current source**, **NOT** taught by Ravon. Moreover, the Examiner acknowledges that the current source is constant in the Office Action, at page 7 "since the current I is constant, the current flowing through M2 will be equal to the current flowing through M1." The Applicant is now claiming a switched current source, which was claimed indirectly in the claims previously with the claimed charge injection. Ravon fails to teach a switched current source, as acknowledged by the Examiner.

The Examiner equates "no current I flow into load C'.2 from current source 11, and charge injection flowing to the load is reduced" (Office Action, page 7). **AGAIN**, the Examiner is ignoring a term of art. Elimination of current flow is **NOT** a reduction of charge injection, as claimed by claims 1-5, 8-10, 12-14, 18, 19, 21 and 22.

Accordingly, for at least all the above reasons, claims 1-5, 8-10, 12-14, 18, 19, 21 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 6, 7 and 11 over Ravon in view of AAPA

In the Office Action, claims 6, 7 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Ravon in view of Applicant's Admitted Prior Art Fig. 3 (AAPA). The Applicant respectfully traverses the rejection as follows.

Claims 6, 7 and 11 are dependent on claim 1, and are allowable for at least the same reasons as claim 1 is allowable.

Claims 6, 7 and 11 recite, *inter alia,* a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered.

As discussed above, Ravon fails to teach a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered, as claimed by claims 6, 7 and 11.

The Office Action correctly acknowledged that Ravon fails to teach a serial combination of transistors. The Office Action relies on AAPA to make up

for the deficiencies in Ravon to arrive at the claimed invention. The Applicant respectfully disagrees.

AAPA teaches an unsatisfactory circuit for reducing charge injection which uses a serial combination of transistors forming a compensating switch (AAPA, Fig. 3). AAPA fails to teach reduction of charge injection by a pull-down mirror path, as claimed by claims 6, 7 and 11.

AAPA and Ravon, either alone or in combination, fail to disclose, teach or suggest, a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered, as claimed by claims 6, 7 and 11.

Accordingly, for at least all the above reasons, claims 6, 7 and 11 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-5, 8-10, 12-14, 18 and 19 in view of Harston

In the Office Action, claims 1-5, 8-10, 12-14, 18 and 19 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over US Patent No. 5,343,196 to Harston ("Harston"). The Applicant respectfully traverses the rejection as follows.

Claims 1-5, 8-10, 12-14, 18 and 19 recite, *inter alia,* a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered.

Harston teaches a method of reducing the amount of current switched to a reference line so as to reduce the overall power consumption of a digital to analog converter (DAC). To achieve this, three transistors are employed. One MOS transistor acts as a current source. The two other transistors act alternatively to direct current to either a load or alternately to ground (Harston, col. 1, line 41-42). The current directed to ground performs no useful purpose (Harston, col. 1, lines 20-23).

AGAIN, the Examiner is ignoring a term of art, i.e., charge injection. Harston is unconcerned with reducing current variations associated with a switched current source. Harston simply changes the state of a DAC as either

receiving current from a source or not receiving current from a source. Harston alternate path to ground performs no useful purpose. Harston alternate path to ground does not reduce charge injection, much less teach a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered, as claimed by claims 1-5, 8-10, 12-14, 18 and 19.

Accordingly, for at least all the above reasons, claims 1-5, 8-10, 12-14, 18 and 19 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 6, 7 and 11 over Harston in view of AAPA

In the Office Action, claims 6, 7 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Harston in view of AAPA. The Applicant respectfully traverses the rejection as follows.

Claims 6, 7 and 11 are dependent on claim 1, and are allowable for at least the same reasons as claim 1 is allowable.

Claims 6, 7 and 11 recite, *inter alia,* a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered.

As discussed above, Harston fails to teach a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered, as claimed by claims 6, 7 and 11.

As discussed above, AAPA fails to teach a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered, as claimed by claims 6, 7 and 11.

Harston and AAPA, either alone or in combination, fail to disclose, teach or suggest a pull down mirror path to reduce charge injection during **switching** of a current source while the current source remains powered, as claimed by claims 6, 7 and 11.

Accordingly, for at least all the above reasons, claims 6, 7 and 11 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Response to the Examiner's Numbered Arguments

The Applicant is responding to the numerical Arguments on pages 15-24 of the Office Action with respective numerical responses.

Response #1

The Office Action again alleges the labeling of switches on page 7, lines 18 and 19 of the specification are incorrect. The Examiner alleges that the current level on the source side of switch MC is considered equal to the current level on the drain side of the switch MC. Since the Examiner believes this to be true, the Examiner does not understand how the Applicant equalizes the current on both ends of the current source MC.

As discussed above, the labeling of the switches on page 7, lines 18 and 19 of the specification is **correct**. A current spike is produced at a switched current source during switching. The Examiner's statement that the current level at the source and drain are at equal levels is true after a short amount of time after the current naturally equalizes. However, during the short period of time during initial switching, a current spike, i.e., charge injection, is produced by the switching circuit. The Examiner is ignoring the claims being addressed to this short period of time when a current spike is produced during switching.

The Examiner alleges that switch MC is shown as a constant current source due to the reference voltage applied to its gate. The Applicant respectfully disagrees.

Switch MC is **NOT** biased by a reference voltage. Switch MC is biased by a bias voltage that controls switching. Switching creates varying currents, **not** addressed by the prior art as discussed above.

Response #2

The Examiner is questioning if the Applicant is considering switch MC as the current source, **or** the combination of MC and MS as the current source (Office Action, page 16). If switch MC is the current source, the Examiner alleges that the current flowing though the source would obviously be equal on both sides of the transistor MC. The Applicant respectfully disagrees.

The Applicant has stated herein and in previous responses that switch MC, and as stated within the specification, is the switched current source. From the Examiner's statement that current is equal on both sides of the transistor, the Examiner is **again** seems to misinterpreting the invention. The Applicant is claiming charge injection, which occurs during the short period of time after switching of a switched current source. The Examiner is stating obvious characteristics when the switched current source reaches a steady state operation. The Examiner is **again** ignoring a claimed recitation, i.e., charge injection. Charge injection is a result of a **switched** current source, **not** a steady state current source produced by a steady state switch.

Response #3

The Examiner alleges that the language a "load substantially continuously receives said current flowing from the current" is not supported by the disclosure. The Applicant respectfully disagrees.

The Examiner is making a 112 paragraph rejection without formally placing it in a section under 112 paragraph rejections. Also, this is a new grounds of rejection that the Applicant has not had an opportunity to address, making the Finality of the rejection improper.

Moreover, the specification details at, e.g., page 2, lines 1-18, that charge injection occurs for a short period of time after switching of a MOS current switch. Since the charge injection is reduced by a pull-down mirror path for a very short period of time, i.e., immediately after switching. The load substantially continuously receives current from the switched current source after charge injection is reduce and current flow is restored to the load.

Response #4

The Examiner alleges that it is not understood why the prior art references will not have reduced charge injection since they switch current flow to, and away from, the load as well (Office Action, pages 18 and 19). Therefore, the Examiner alleges that a broad interpretation of the claims allows the claims to read on cited prior art.

As the Applicant **repeatedly** stresses, and the Examiner **repeatedly** ignores, the Applicant is claiming a term of art, i.e., charge injection.

As the Applicant has repeatedly stated and the Examiner has repeatedly ignored, charge injection is a term of art having a definition within the art. Charge injection is a current spike that occurs when, e.g., a MOS switch is switched from an OFF state to an ON state. The prior art fails to teach a reduction of charge injection, as claimed by all the pending claims.

The Examiner again seems to be misinterpreting the term of art by incorrectly defining charge injection as simply a switching a current source to and away from a load. Charge injection is associated with a current spike related to a switched current source, **still not addressed** by the Examiner.

Response #5

The Examiner alleges that Ravon teaches a reduction of charge injection by eliminating transients in voltage within the circuit while maintaining a constant current. The Examiner alleges that charge injection is related to the switching operation within the circuit (Office Action, page 19). The Applicant respectfully disagrees.

Again, the Examiner is either ignoring or misinterpreting a term of art, i.e., charge injection. As discussed above, charge injection is associated with a current spike related to a switched current source, NOT simply switching operations within a circuit.

Moreover, the Examiner **acknowledges** Ravon teaches a constant current. Charge injection is a current spike, **NOT** a constant current. Ravon fails to address the problem of a current spike associated with a switch current source.

Response #6

The Examiner alleges the Applicant is relying on features for patentability that are not recited within the claims. In particular, the Examiner alleges that the current source is switched on and off was not recited within the claims. The Applicant respectfully disagrees.

Charge injection is a term of art, i.e., a current spike produce when a current source is switched on and off. To help clarify this feature of charge injection, the Applicant has added limitation to the claims. Although this feature

is now in the claims, the claims had indirectly recited this limitation by a recitation of charge injection.

Response #7

The Examiner alleges that since the cited prior art references teach similar circuitry, but do not specifically state a reduction of charge injection, charge injection reduction is inherently taught by the references. The Applicant respectfully disagrees.

The Examiner equates a reduction of charge injection to a simply diverting a current source's current away from a load (Office Action, pages 21 and 22).

AGAIN, the Examiner is ignoring a term of art, i.e., charge injection that is a current spike produced when a current source switch is turned switched. Simply diverting a current source's current shows the Examiner either is ignoring a term of art or misinterpreting the invention.

Response #8

The Examiner alleges that Applicant wants to claim the invention broadly, but then the prior art must be narrowly interpreted. However, this reasoning does not correspond to the knowledge of one of ordinary skill in the art (Office Action, page 23).

If the Examiner is relying on the Examiner own knowledge, the Examiner must submit an affidavit supporting his knowledge. Otherwise, the Examiner must rely on the teachings within the prior art cited, which fails to teach a reduction of charge injection during switching of a current source, as claimed.

Response #9

The Examiner alleges that since the AAPA teaches a circuit to reduce charge injection and the cited prior art teaches a pull-down mirror path, the references can not be attacked individually.

The Applicant is **not** attacking the references individually. If neither of the references teach a claim limitation, a combination of the two reference **can not** teach the claim limitation.

AAPA teaches a reduction of charge injection. Applicant is not making the allegation that not one has ever attempted to reduce charge injection.

On the contrary, the AAPA teaches an unsatisfactory attempt to reduce charge injection. The cited references do not address charge injection, but diverting current from a load. Combining the cited prior art with AAPA creates a circuit that unsatisfactorily reduces charge injection and diverts current from a load. At best, the combination could not produce a pull-down mirror path to reduce charge injection during switching of a current source.

The Examiner's cited prior art fails to even contemplate a reduction of charge injection for their disclosed circuits.

Response #10

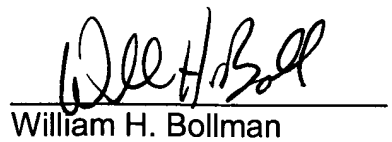
The Examiner alleges Applicant amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The Examiner alleges confusion related to the claim language (Office Action, page 24).

The Applicant specifically addressed what Ravon and Harston teach. The Applicant specifically addressed what was claimed and how the cited prior art fails to disclose, teach or suggest the claimed limitations. Moreover, the confusion related to the claim language **again** remains with the Examiner, since the Examiner is ignoring a term of art, i.e., charge injection. The Examiner is taking a term of art and applying a definition created by the Examiner. There is no confusion within the art as to a definition of charge injection.

Conclusion

All rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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Version with Markings to Show Changes Made

1. (Four Times Amended) A current source switching circuit with reduced charge injection, comprising:

a current source;

a transistor switch;

a pull-down mirror path in parallel with said transistor switch operating to equalize a current level produced by said current source; and

a first load;

wherein said transistor switch and said pull-down mirror path operate to substantially continuously reduce said charge injection flowing to said first load during switching of said current source while said current source remains powered.

18. (Four Times Amended) A method of reducing charge injection from a current source through a current switch into a load, said method comprising:

providing a pull-down mirror path in parallel with said current switch, said pull-down mirror path and said current switch operating to equalize a current level produced by said current source;

turning a switch in said pull-down mirror path on when said current switch is turned off; and

turning said switch in said pull-down mirror path off when said current switch is turned on;

wherein said current switch and said pull-down mirror path operate substantially continuously to reduce said charge injection flowing to said load during switching of said current switch while said current source remains powered.

21. (Three Times Amended) A method of switching a current source out from a load, said method comprising:

opening a transistor switch connecting said current source to said load; and

substantially simultaneously with said step of opening, closing a switch to a pull-down mirror path in parallel with said transistor switch so that current from said current source flows through said pull-down mirror path, said pull-down mirror path and said transistor switch operating to equalize a current level produced by said current source;

wherein said load substantially continuously receives said current flowing from said current source to reduce charge injection from said current source to said load during switching of said current source while said current source remains powered when said transistor switch is opened.

22. (Three Times Amended) Apparatus for switching a current source out from a load, comprising:

means for opening a transistor switch connecting said current source to said load; and

means for closing a switch to a pull-down mirror path in parallel with said transistor switch at substantially simultaneously a same time as said means for opening opens said transistor switch so that current from said current source flows through said pull-down mirror path, said pull-down mirror path and said transistor switch operating to equalize a current level produced by said current source;

wherein said load substantially continuously receives said current flowing from said current source and charge injection is reduced from said current source to said load during switching of said current source while said current source remains powered when said transistor switch is opened [is reduced].